50. A system according to claim 48 and further comprising at least one FIFO unit used by said first CPU and said second CPU to transfer data therebetween.

51. A system according to claim 48 wherein said communications means is able to process networking protocol commands.

52. A chip comprising instructions for at least two processing units embedded on said chip to asynchronously control reading and writing of data to and from memory on said chip.

53. A chip comprising instructions for at least two processing units embedded on said chip to generally independently control access to data from memory on said chip.